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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,512	03/29/2001	David William Boerstler	AUS920000511US1	5447

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EXAMINER	
TSE, YOUNG TOI	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,512	BOERSTLER, DAVID WILLIAM	
	Examiner	Art Unit	
	YOUNG T. TSE	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,12-14 and 24* is/are rejected.

7)☒ Claim(s) *3-11 and 15-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *032901*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 17-19, filed December 03, 2004, with respect to the rejection(s)of claim(s) 1-12 under 35 U.S.C. 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Buckner et al., Lee et al. (both were cited by the examiner in the last Office Action) and Ducaroir et al..

Drawings

2. The drawings were received on December 03, 2004. These drawings are acceptable.

Specification

3. The disclosure is objected to because of the following informalities: on page 6, line 19, "generation" should be "generator". Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Buckner et al. (was cited in the last Office Action)

Buckner et al. (US Patent No. 5,509,037) discloses a receiver circuit in Figure 2 comprising a plurality of phase alignment circuits 34 for aligning a plurality of serial data with a plurality of clock phases generated from a phase locked loop (PLL) circuit 30 of an internal clock to generate retiming data to a switching matrix 36.

Figure 3 shows the detailed embodiment of the PLL circuit 30 for generating the plurality of the clock phases.

Figure 4 shows the waveforms of the plurality of clock phases, the input of the serial data, and the retiming data of the serial data.

Figure 5 shows the detailed embodiment of one of the plurality of the phase alignment circuits 34 comprising a retiming circuitry 37 and a slip buffer 38.

The retiming circuitry 37 includes an asynchronous data capturer 40 for receiving the serial data and the phases of the internal clock, a data transition decoder 44 for performing the task of determining the occurrence of the data transition with respect to the plurality of clock phases, and a data timer 50 for realigning the captured data of one of the plurality of the clock phases. See column 4, lines 14-41 and column 5, lines 31-34.

The detailed embodiment of both the asynchronous data capturer 40 and the data transition decoder 44 is shown in Figure 6a and the detailed embodiment of the data timer 50 is shown in Figures 6b and 6c.

The slip buffer 38 includes a forward/backward decoder 56, a state machine 58, and a data path selector 64.

The detailed embodiment of the forward/backward decoder 56, the state machine 58, and the data path selector 64 is shown in Figures 7a and 7b.

With respect to claim 1, the phases of the internal clock are generated by the voltage controlled oscillator (VCO) 43 of the PLL circuit 30; the retiming circuit 34 includes the asynchronous data capturer 40 for receiving the serial data and the phases of the internal clock and the data transition decoder 44 the data timer 50 which may also includes the data path selector 62 operable to reduce timing uncertainties in the serial data by outputting a value of the serial data sampled at a particular phase of the internal clock. Wherein each data phase alignment circuitry 34 receives phases Φ1- Φ5 of the clock signal, the serial data, and aligns the data with a selected phase of the clock signal. See column 3, lines 34-36.

With respect to claim 2, the data generated by the data timer 50 corresponds to a particular retiming state, which may be generated, for example, by the CMOS transmission gates 120-128. See column 5, lines 4-8.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buckner et al. in view of Ducaroir et al..

With respect to claims 13 and 14, Buckner et al. discloses all the claimed subject matter as discussed in paragraph 5 above. However, Buckner et al. fails to show or suggest that the receiver circuit receives the serial data from a transmission medium transmitted by a transmitter comprising a parallel to serial converter for converting the serial data to the transmission medium.

Ducaroir et al. (U.S. Patent No. 6,331,999 B1) discloses a serial data transceiver circuit 59 in Figure 7 comprising a transmitter circuit having a parallel to serial converter to convert a parallel input data to a serial data stream and a receiver circuit to receive the serial data stream to parallel output, recover a transmit clock signal used to transmit the serial data from the serial data stream to generate a timing signal based upon the recovered transmit clock, samples the serial data stream using the timing signal in order to recover the data stream from the serial data stream, align the serialized data into

parallel units, and provide the resulting parallel data at the received data output port. See the abstract.

Therefore, it would have been obvious to one of ordinary skill in the art that the serial data received in Buckner's receiver circuit is transmitted from a parallel to serial converter circuit of a transmitter through a transmission medium in order to recover a transmitted clock by a receiver as taught by Ducaroir.

9. Claims 12 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buckner et al. in view of Lee et al. (was cited in the first Office Action).

As applied to claim 1 and claim 13 discussed in paragraphs 5 and 8 above. Although Buckner does not show or suggest the relationship of the data rate between the serial data and the clock signal that the oscillator 43 operates at a frequency lower than a data rate of the serial data. It appears to be well known to a person skill in the art that the frequency generated from one of the phases Φ1- Φ5 by the oscillator 43 is lower than the data rate of the serial data since the oscillator 43 has divided the internal clock into five different clock phases.

Even it is not well known to a person skill in the art as discussed above, Lee et al. (U.S. Patent No. 6,266,799) discloses a data/clock recovery system 100 in Figure 1 comprising a transmitter circuit 108 for transmitting a serial data to a receiver circuit 110 through a transmission medium.

Figure 2 shows the detailed embodiment of the receiver circuit 110 having a multi-phase clock generator 204 for generating a plurality of clock phases, a multi-phase

data clock recovery unit 110a for recovering the serial data and the plurality of clock phases into recovery clocks and data to a serial to parallel converter 206.

Lee teaches that the data and recovered clock provided to the serial to parallel converter 206 will be processed at a much lower rate than the data baud rate to produce synchronized data and clock before the data is transferred to the media access control (MAC) 102 circuitry. See column 5, lines 52-58.

Therefore, it would have been obvious to one of ordinary skill in the art to generate a frequency in Buckner's oscillator 43 lower than the data rate of the serial data as taught by Lee for the purpose of saving power or synchronize data and clock before the data is transferred to other circuitry.

Allowable Subject Matter

10. Claims 3-11 and 15-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to show or suggest that a retiming circuit includes circuitry for generating pairs of synchronization states and retiming states to indicate which particular phase of the clock to assert at a given transition of the serial data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday and Wednesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YOUNG T. TSE
Primary Examiner
Art Unit 2637